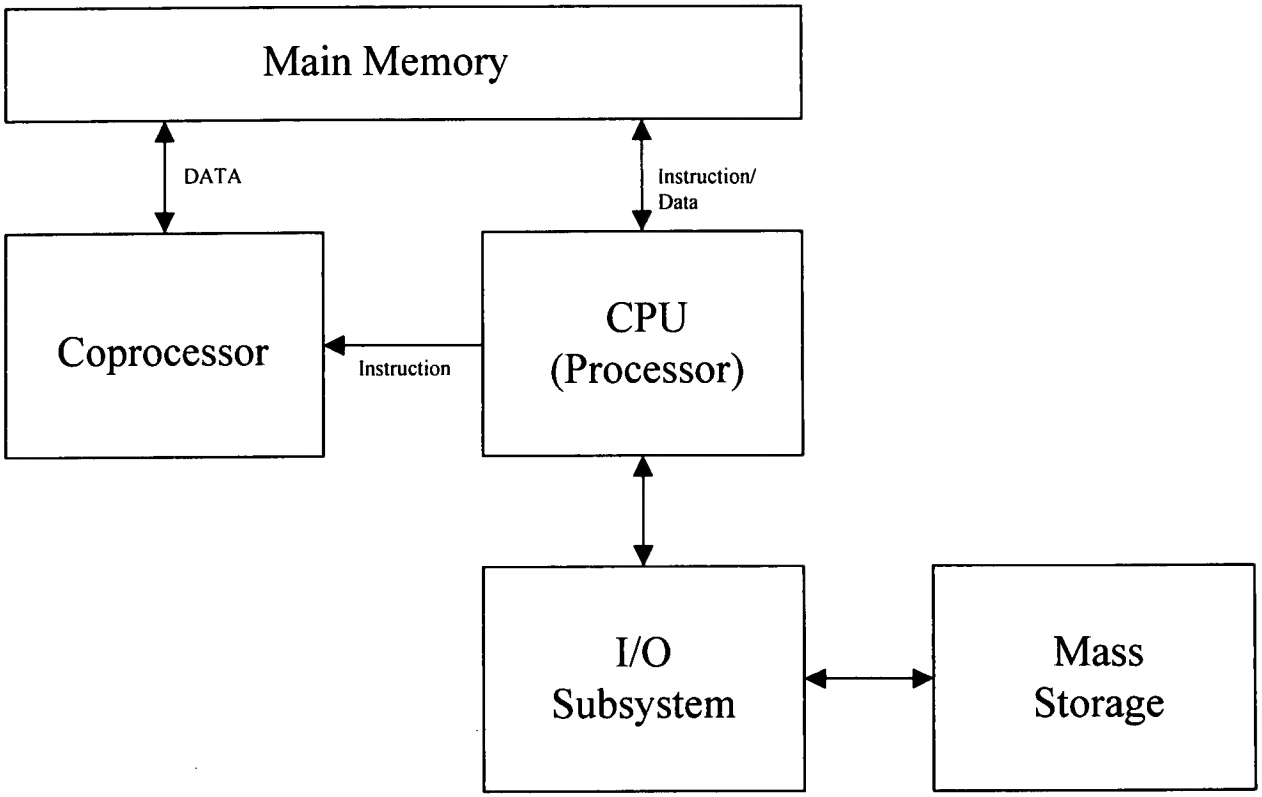

FIG. 1
(PRIOR ART)

Coprocessor	Compatible Processor	Coprocessor Characteristics
Intel 8087	Intel 8086/8088	5 Mhz, 70 cycles for add & 700 cycles for log
Intel 80287	Intel 80286	12.5 Mhz, 30 cycles for add & 264 cycles for log
Intel 387DX	Intel 386DX	33 Mhz, 12 cycles for add & 210 cycles for log
Intel i486	Intel i486 (same chip)	33 Mhz, 8 cycles for add & 171 cycles for log
Motorola MC68882	Motorola MC68020/68030	40 Mhz, 56 cycles for add & 574 cycles for log
Weitek 3167	Intel 386DX	33 Mhz, 6 cycles for add & 365 cycles for log by software emulation
Weitek 4167	Intel i486	33 Mhz, 2 cycles for add & not available for log

FIG. 2
(PRIOR ART)

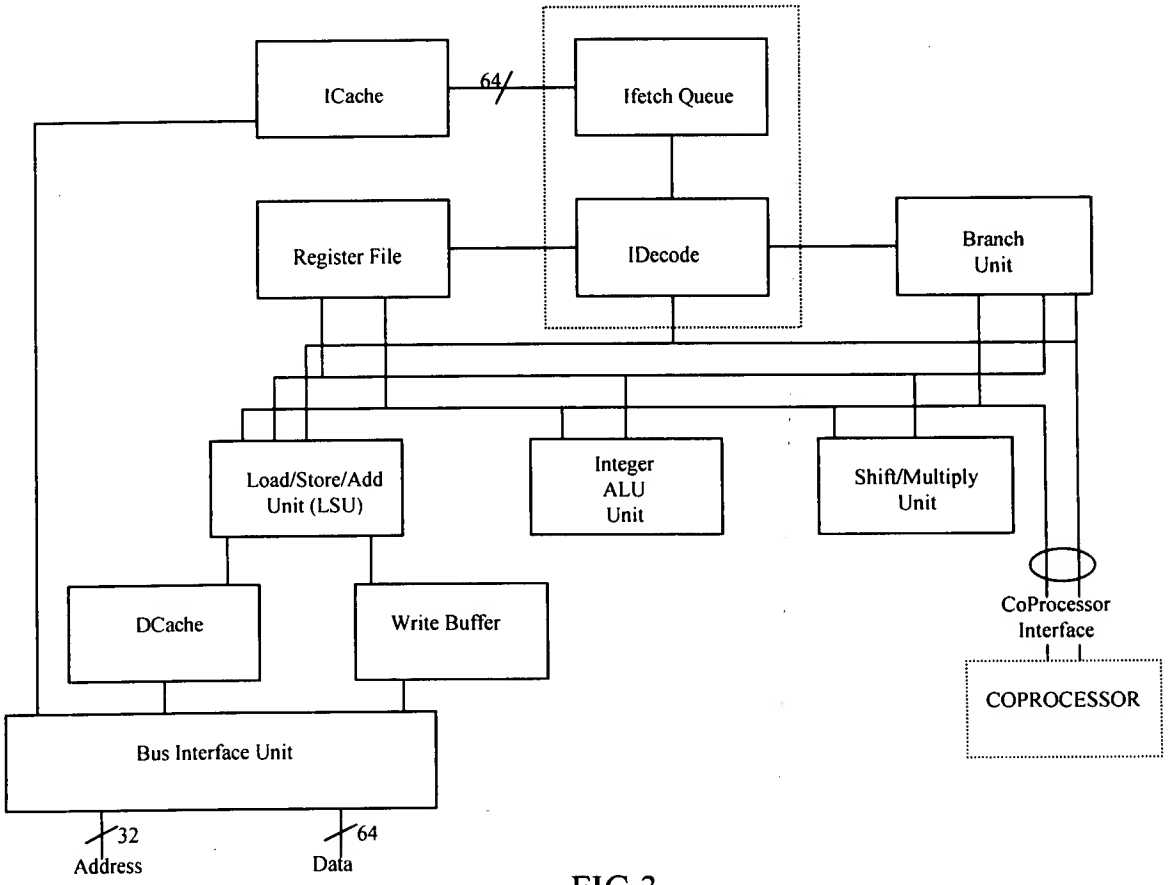

FIG.3
(PRIOR ART)

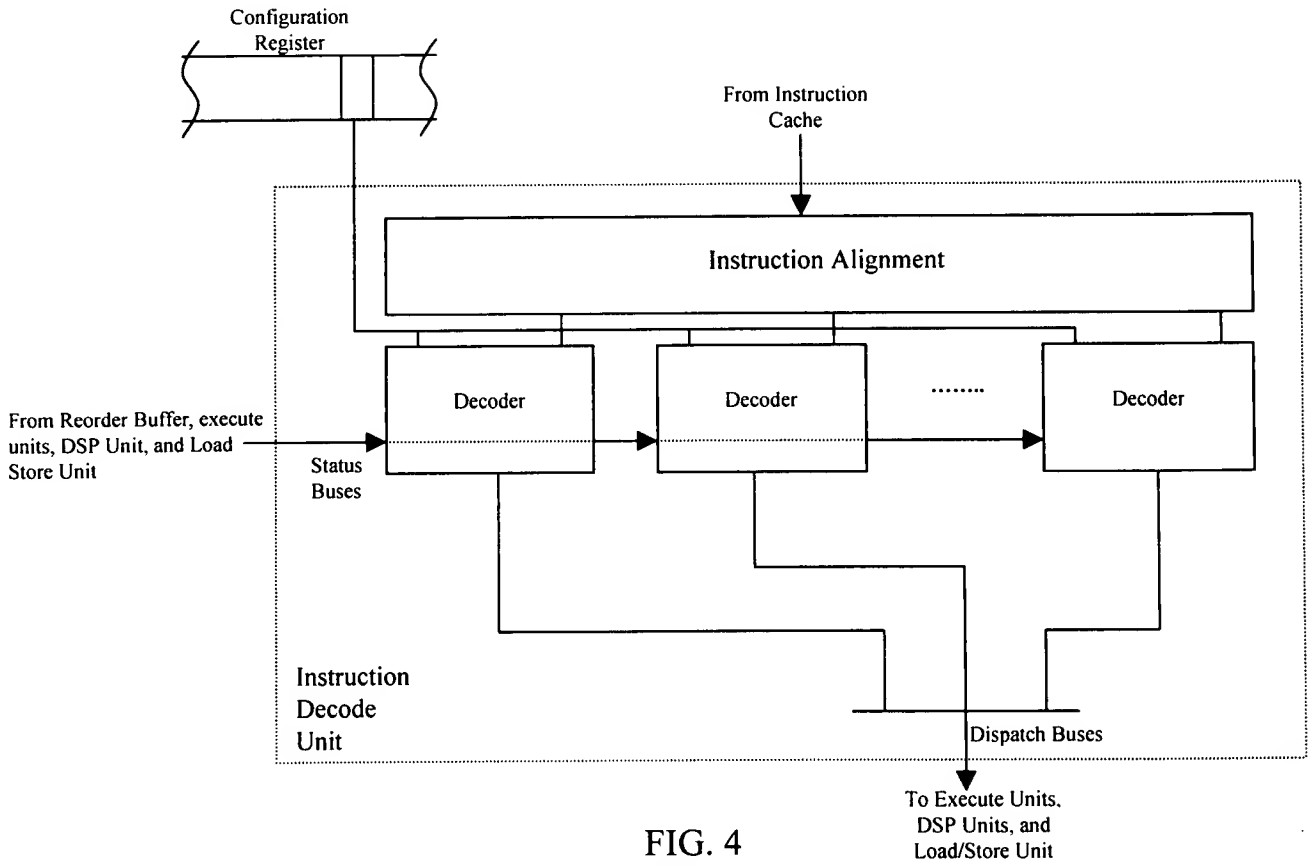

FIG. 4
(PRIOR ART)

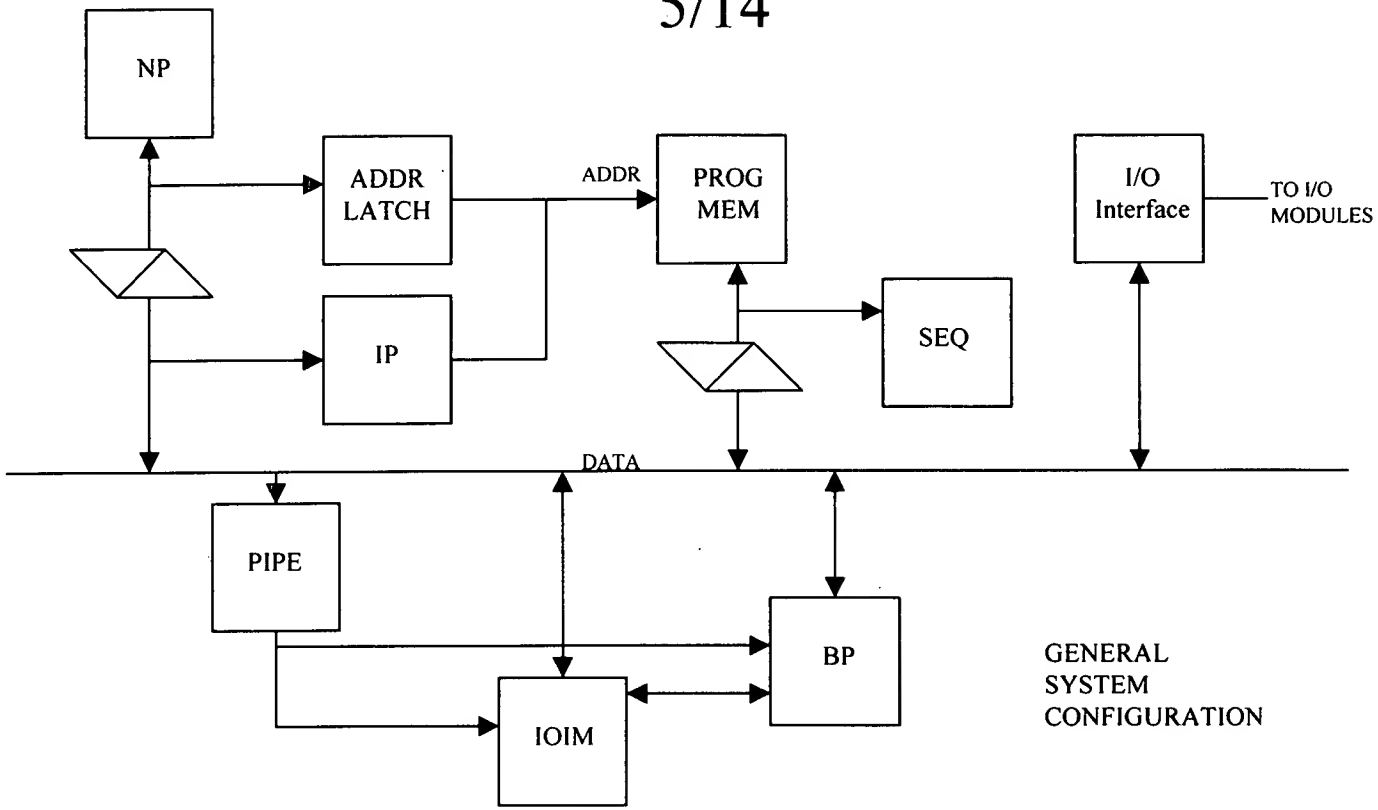

FIG. 5
(PRIOR ART)

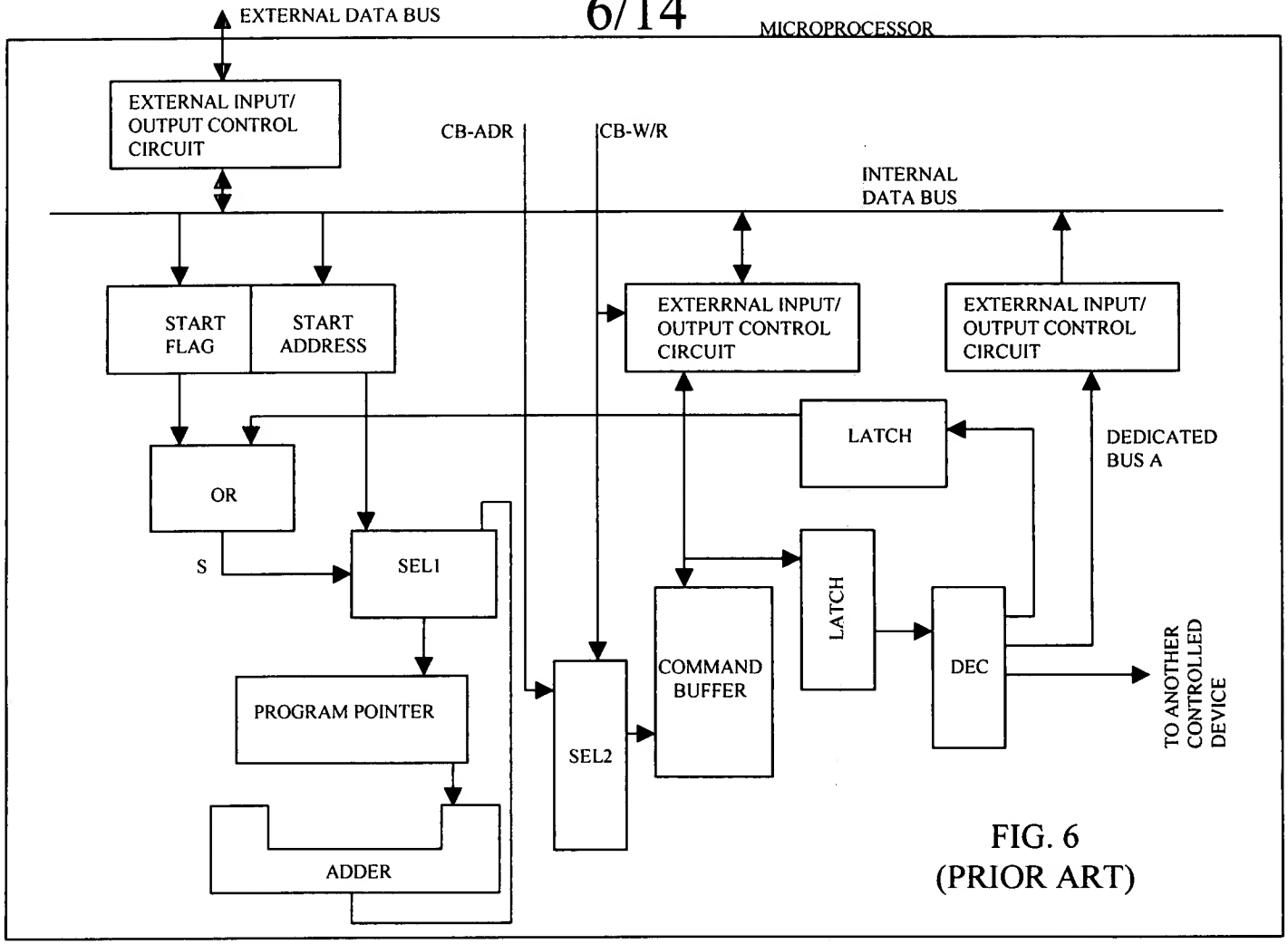

FIG. 6
(PRIOR ART)

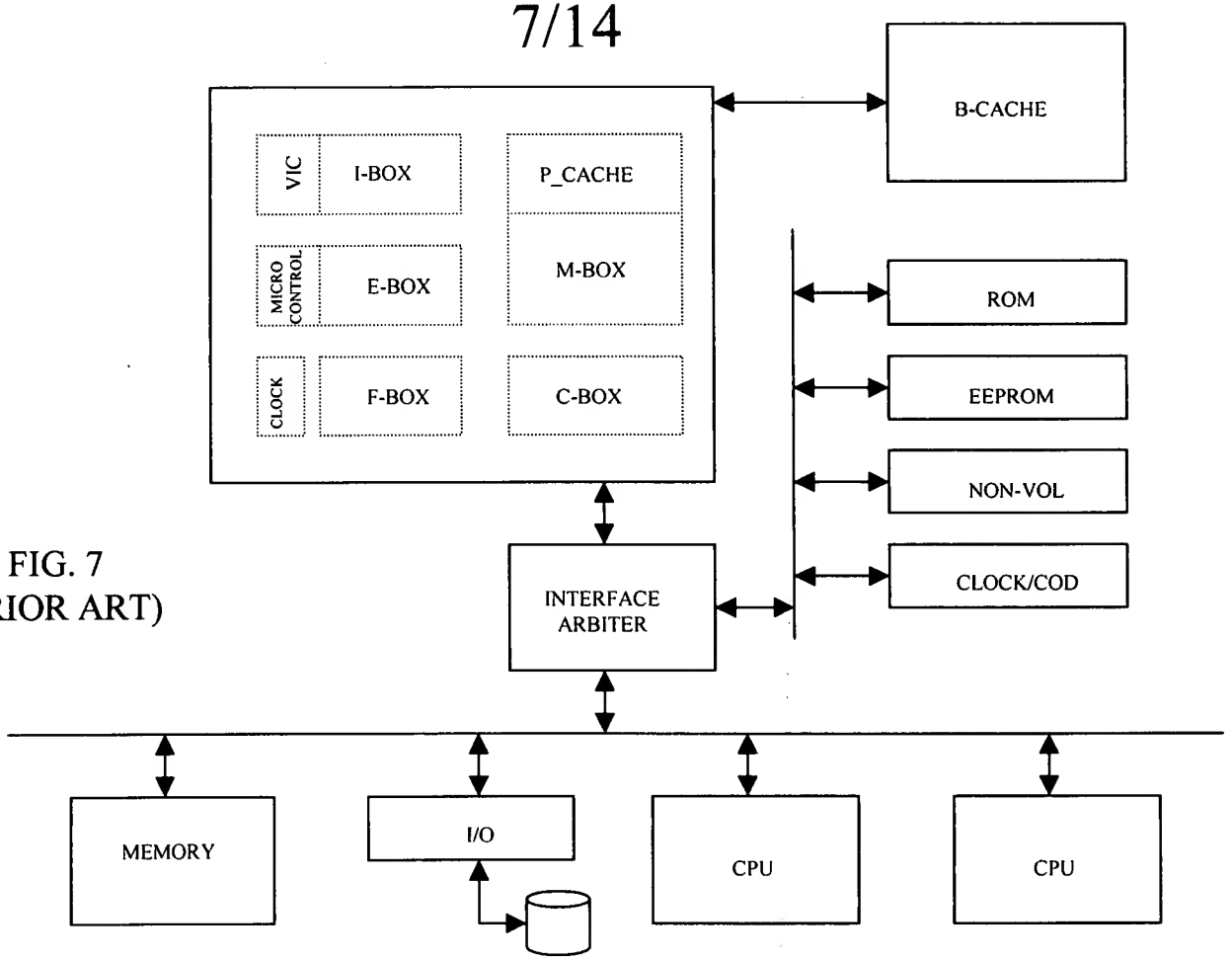

FIG. 7
(PRIOR ART)

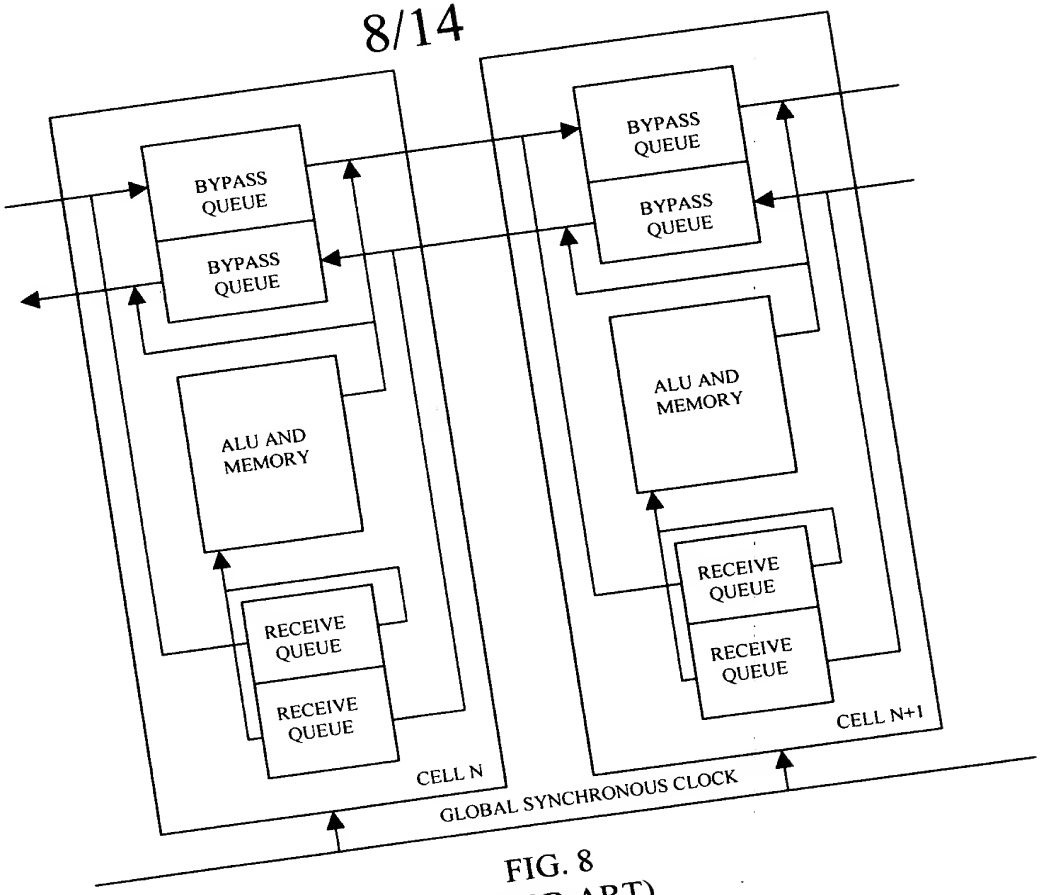

FIG. 8
(PRIOR ART)

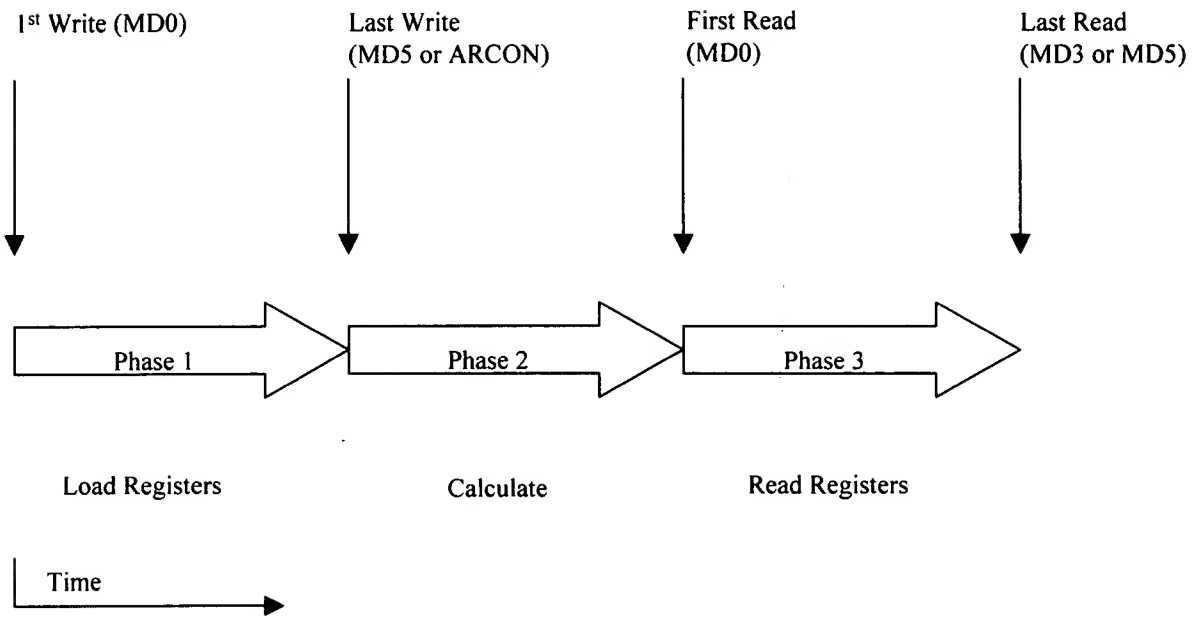

FIG. 9
(PRIOR ART)

Operation	Result	Remainder	Execution Time
32-bit/16-bit	32-bit	16-bit	6 tcy
16-bit/16-bit	16-bit	16-bit	4 tcy
16-bit x 16-bit	32-bit	-	4 tcy
32-bit normalize	-	-	6 tcy
32-bit shift left/right	-	-	6 tcy

Notes:
1) 1 tcy = 1 microsecond at 12 Mhz Oscillator frequency
2) The maximum shift speed is 6 shifts per machine cycle

FIG. 10
(PRIOR ART)

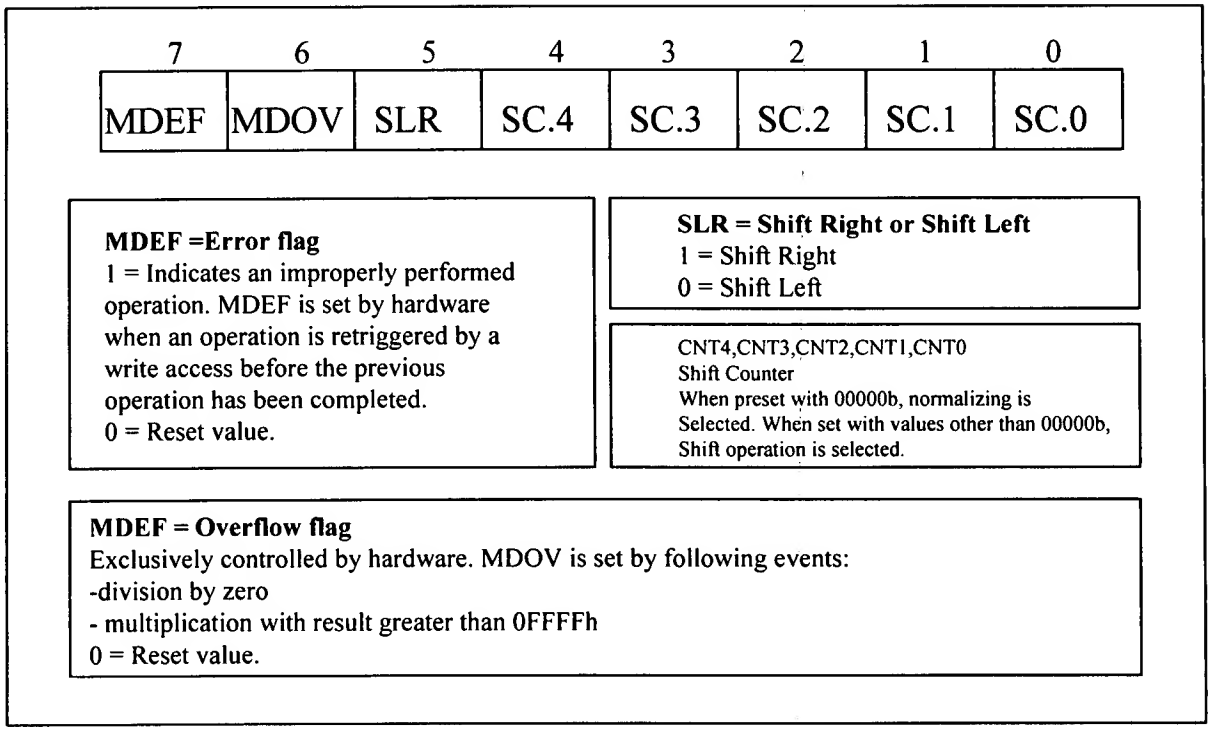

FIG. 11
(PRIOR ART)

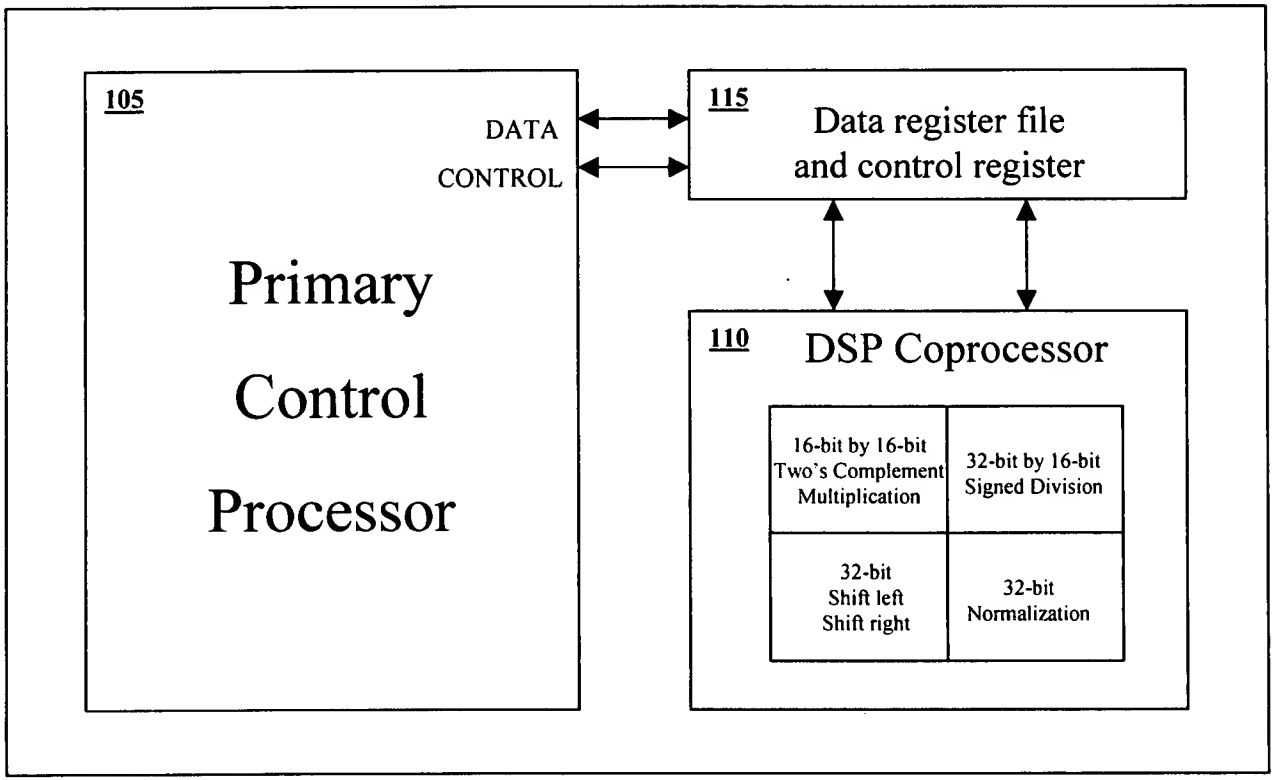
105
DATA
CONTROL
Primary
Control
Processor
115
Data register file
and control register
110
DSP Coprocessor
16-bit by 16-bit
Two's Complement
Multiplication
32-bit by 16-bit
Signed Division
32-bit
Shift left
Shift right
32-bit
Normalization

FIG. 12

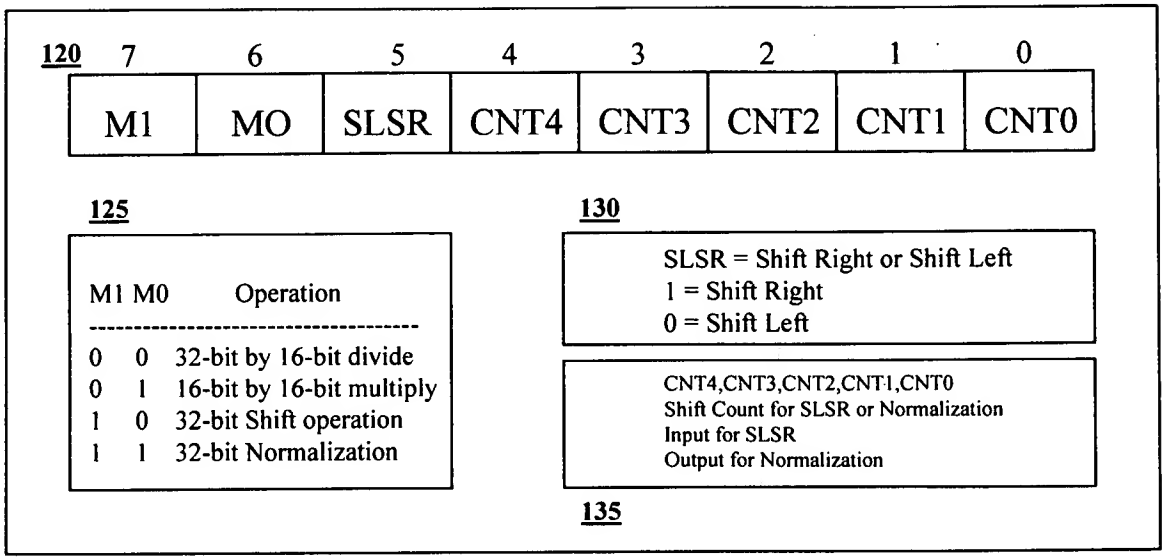
120
7 6 5 4 3 2 1 0
M1 MO SLSR CNT4 CNT3 CNT2 CNT1 CNT0
125
M1 M0 Operation
0 0 32-bit by 16-bit divide
0 1 16-bit by 16-bit multiply
1 0 32-bit Shift operation
1 1 32-bit Normalization
130
SLSR = Shift Right or Shift Left
1 = Shift Right
0 = Shift Left
CNT4,CNT3,CNT2,CNT1,CNT0
Shift Count for SLSR or Normalization
Input for SLSR
Output for Normalization
135

FIG. 13

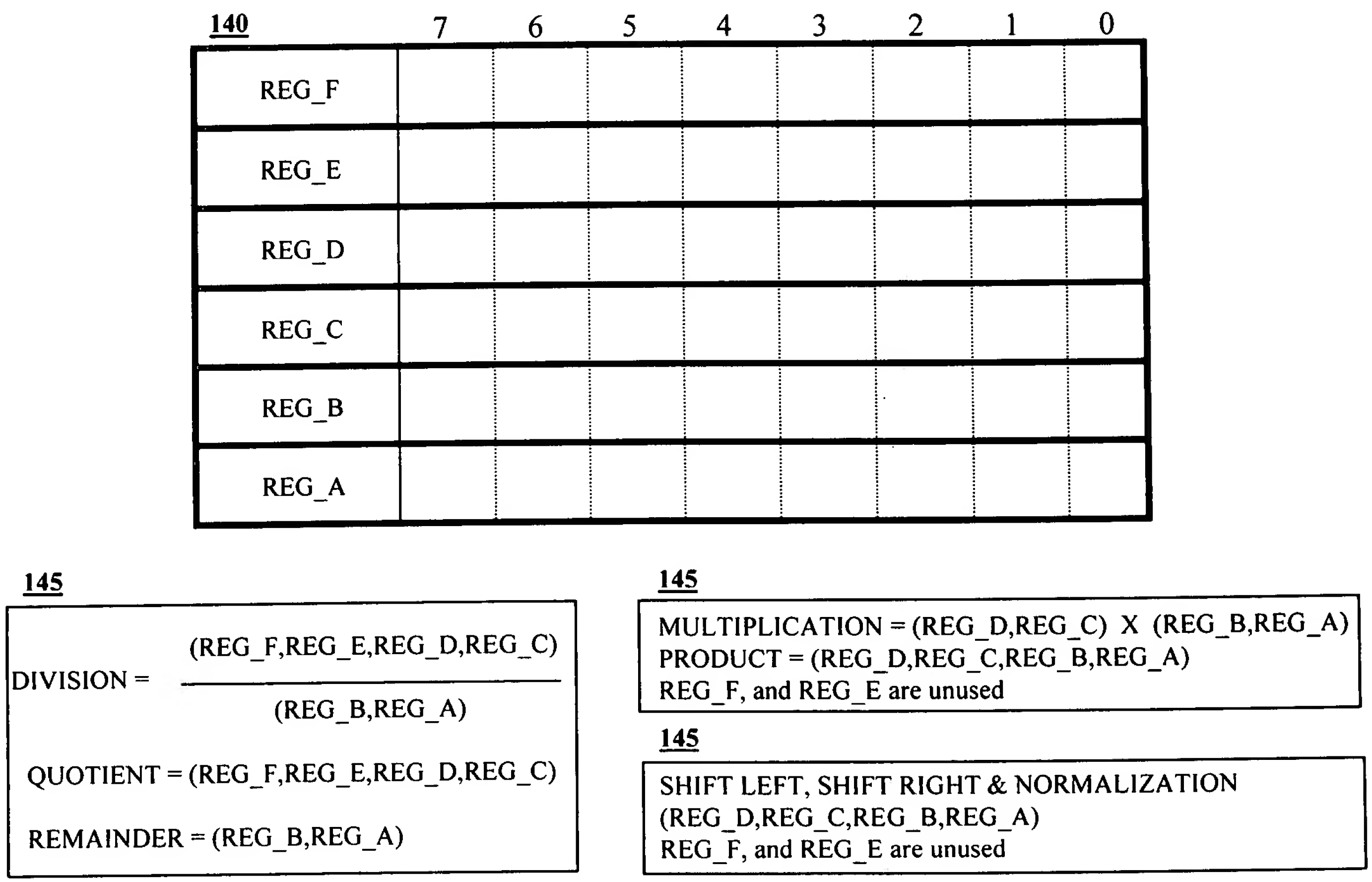
140
7
6
5
4
3
2
1
0
REG_F
REG_E
REG_D
REG_C
REG_B
REG_A
145
DIVISION = (REG_F,REG_E,REG_D,REG_C) / (REG_B,REG_A)
QUOTIENT = (REG_F,REG_E,REG_D,REG_C)
REMAINDER = (REG_B,REG_A)
145
MULTIPLICATION = (REG_D,REG_C) X (REG_B,REG_A)
PRODUCT = (REG_D,REG_C,REG_B,REG_A)
REG_F, and REG_E are unused
145
SHIFT LEFT, SHIFT RIGHT & NORMALIZATION
(REG_D,REG_C,REG_B,REG_A)
REG_F, and REG_E are unused

FIG. 14